PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-337047

(43)Date of publication of application : 07.12.2001

(51)Int.Cl. G01N 21/956
H01L 21/66
// G01B 21/30

(21)Application number : 2000-160506

(22)Date of filing : 30.05.2000

(71)Applicant : TOSHIBA CORP

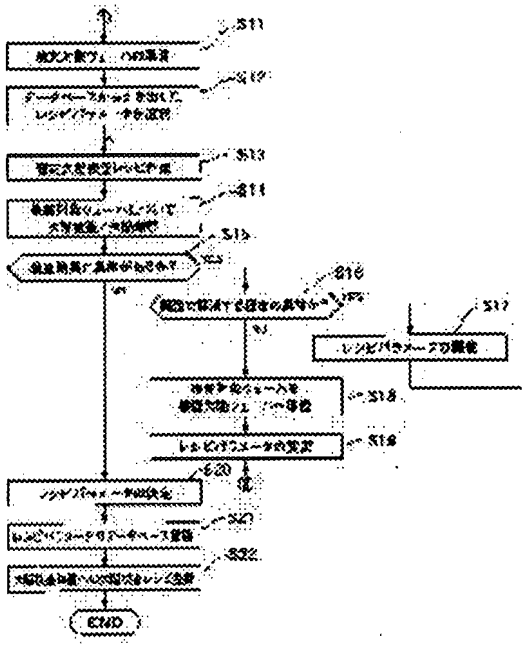
(72)Inventor : NODA TOMONOBU

(54) SIMULATED DEFECT WAFER AND METHOD FOR FORMING DEFECT INSPECTION RECIPE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for forming independently of a proficiency of a former an optimum defect inspection recipe whereby all kinds of defects can be detected.

SOLUTION: A temporary inspection recipe is formed with the use of the simulated defect wafer 1 including simulated defect patterns DF1-DF3 having a change in a height direction and a change in a plane shape to a simulation normal pattern. Defect inspection of the simulated defect wafer 1 is carried out. Detected defect data are compared with preliminarily obtained simulated defect data of the simulated defect wafer 1 to quantify a defect detection sensitivity. Recipe parameters are changed until a desired defect detection rate is obtained. The temporary inspection recipe is thus formed.



LEGAL STATUS

[Date of request for examination] 24.06.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number] 3735517

[Date of registration] 28.10.2005

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention is aimed at the simulation defective wafer and the defective inspection recipe creation approach of using for semi-conductor defective inspection about semi-conductor defective inspection.
[0002]
[Description of the Prior Art] An example of the creation approach of the defective inspection recipe by the Prior art is explained referring to the flow chart of drawing 14 .
[0003] First, the wafer used as a subject of examination is prepared (step S91), next the parameter for recipes is chosen provisionally (step S92), and a provisional inspection recipe is created (step S93). Next, the defect which inspected the wafer to be examined actually and was detected is observed (step S94), and the defective detection sensitivity by the provisional inspection recipe judges whether desired detection sensitivity is reached from the class (henceforth a defective kind) of the defect, or the magnitude of a defect (step S95). When it is judged that desired detection sensitivity is not reached, a series of procedures of selection of a recipe parameter, creation of a provisional inspection recipe, wafer inspection, and defective observation are repeated until it fills desired detection sensitivity (steps S92-S95). When it is judged that desired detection sensitivity was reached, the recipe parameter chosen at the end is determined as a checking recipe parameter (step S96), it registers to defective test equipment by making the provisional inspection recipe at that time into a defective inspection recipe (step S97), and inspection recipe creation is ended.
[0004]
[Problem(s) to be Solved by the Invention] However, there were the following troubles in the conventional inspection recipe creation approach mentioned above.
[0005] That is, since it is a semi-conductor product with a actual wafer and TEG (Test Element Group) to be examined, the defective information what kind of how many defective kinds exist actually cannot be acquired beforehand. For this reason, it has not grasped that all desired defective kinds have detected or other defective kinds cannot be detected or whether it exists at all. Moreover, the problem that it was greatly influenced by an implementer's level of skill also had the quality of an inspection recipe.
[0006] Moreover, even if it was going to use not a actual wafer but the simulation defective wafer, there was only what was created with monolayer structure conventionally. For this reason, only the superficial defective kind has been created like the simulation defect 101,102 shown in drawing 15 . However, as shown in drawing 16 , the defect which may happen actually also has many from which the location in the height directions (direction vertical to a substrate side), such as the defect 103 formed on the pattern and the defect 104 formed in the clearance between the patterns on a substrate, differs, and is difficult for the simulation defective wafer of monolayer structure to realize such a defect.
[0007] This invention is made in view of the above-mentioned situation, and the object is to offer the inspection recipe creation approach that it does not leak and a desired defective kind can be detected, without being dependent on an implementer's level of skill while offering the simulation defective wafer in consideration of various defective kinds of defective checking.
[0008]
[Means for Solving the Problem] This invention aims at solution of the above-mentioned technical problem with the following means.
[0009] That is, according to this invention, it is formed on a semi-conductor substrate and the simulation defective wafer with which it is formed on the simulation normal pattern whose distance of a top face and the front face of the above-mentioned semi-conductor substrate is the 1st die length, and the above-mentioned semi-conductor substrate, and the distance of a top face and the front face of the above-mentioned semi-conductor substrate is equipped with the

1st simulation defective pattern which is the 1st die length of the above and the 2nd different die length is offered.

[0010] The simulation defective wafer which realizes in simulation the defect from which a location differs in the height direction among the defects from which it may arise actually since the distance of the top face of the simulation defective pattern of the above 1st and the front face of the above-mentioned semi-conductor substrate differs from the distance of the top face of the above-mentioned simulation normal pattern and the front face of the above-mentioned semi-conductor substrate is offered. Here, the above-mentioned simulation normal pattern means the pattern which formed in simulation the pattern formed as a design good on the simulation defective wafer on the semiconductor wafer which is a subject of examination.

[0011] As for the above-mentioned simulation defective wafer, it is desirable to have further the 2nd simulation defective pattern which has a flat-surface configuration which is formed on the above-mentioned semi-conductor substrate, and is different from the above-mentioned simulation normal pattern. The defective kind in a flat-surface configuration is also realizable with the simulation defective pattern of the above 2nd.

[0012] If the simulation defective pattern of the above 1st contains the pattern formed on the above-mentioned simulation normal pattern, it is suitable.

[0013] Moreover, the simulation defective pattern of the above-mentioned simulation normal pattern, the above 1st, and the above 3rd may consist of layered products containing the electric conduction film. Thereby, the simulation defective wafer which imitated the defect in a circuit pattern is offered.

[0014] Moreover, the parameter setup process which according to this invention is the creation approach of a recipe file used for semi-conductor defective test equipment, and sets a recipe parameter as arbitration, The 1st provisional recipe creation process which creates the 1st provisional defective inspection recipe based on the above-mentioned recipe parameter, The simulation defective detection process of detecting a defect using the provisional defective inspection recipe of the above 1st about the simulation defective wafer with which the simulation defective data which are data about a defective kind were obtained beforehand, The defective detection ratio calculation process which computes the defective detection ratio of the provisional defective inspection recipe of the above 1st by collating the defective data and the above-mentioned simulation defective data which were detected,